HIGH PERFORMANCE CHIP CARRIER SUBSTRATE

Abstract of the Disclosure

A multilayer chip carrier with increased space for power distribution PTHs and reduced power-related noise. In a multilayer chip carrier with two signal redistribution fanout layers, in addition to signal escape from near-edge signal pads at the first fanout layer, remaining signal pads are moved closer to the edge of the chip footprint. At the voltage layer below the first fanout layer, the remaining signal pads are moved again, closer to the edge of the chip footprint. In the second fanout layer, below the voltage layer, the remaining signal pads escape. The region where signal pads are moved provides increased space for power PTHs.